CHAPTER 7. MAJOR IC INFORMATIONS

[1] MAJOR IC INFORMATIONS

1. General ICs Information

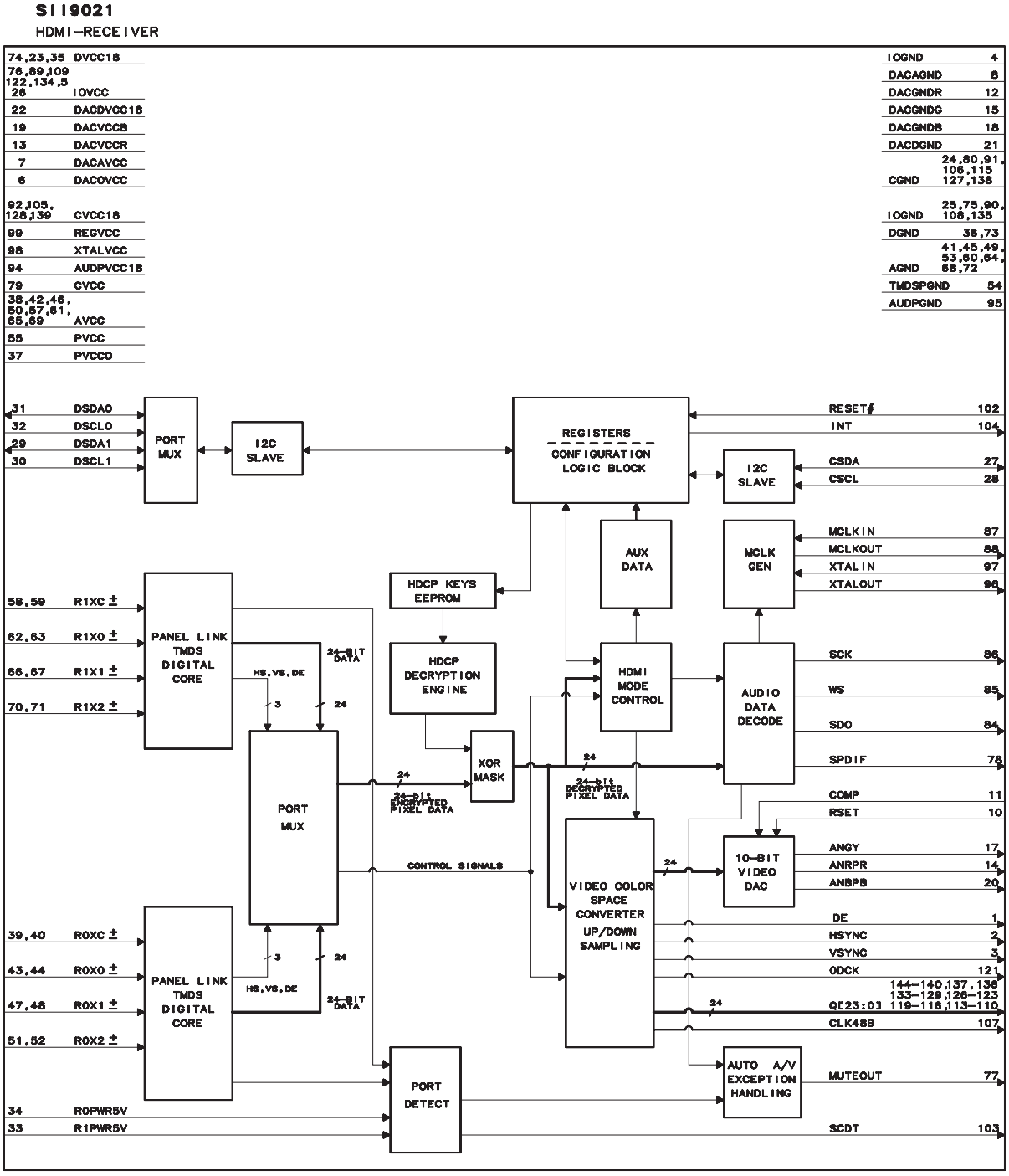
Ref No.	Name	Part Code	Description
KD890FM (MAIN UNIT)			
IC1905 1	HDMI-Receiver	VHISII9021+-1Q	The Sil9021 is a second generation panel Link Cinema receiver that is compatible with the HDMI 1.1 (High Definition Multimedia interface) specification. The Sil9021 is capable of receiving and outputting two channel digital audio at up to 192KHz - an excellent solution for Digital TVs. The feature of this IC is as follows. 1) Digital video interface supports video processors: 2) Analog RGB and YPbPr output: 10-bit DAC. 3) Digital audio interface supports high-end audio systems:
IC2701 2	4CH-MULTIPLEXER	VHITVHC153T-1Y	This IC is a super high speed CMOS 4-channel multiplexer using the CMOS technology and incorporates 2 circuits. The input consists of 2 addresses A, B, 4 channel inputs C0-C3 and strobe input G, and the signal of the channel selected by the address input sent as the output Y. The strobe input is used for prohibition of data output. That means, when G input is “H” the output becomes “L” unconditionally. In this model, this IC operates the switch of H/V-SYNC on each signal condition.
IC3002 3	VIDEO PROCESSOR	RH-IXB624WJN1Q	The VCT 6wxyP family is based on functional blocks contained and approved in existing products like VCT49xxl, VSP 94x5B, and DPS 94xxA. That is, the following 6 major functions are included: 1) Audio Processing 2) Video Processing 3) Motion Adaptive Upconversion 4) Scaling, Display Processing and FPD 5) Unified memory for Audio, Video and Text Control, 3D Combfilter PC Connectivity 6) Controlling, OSD and Text
IC3003 3	Microcontroller	RH-IXB664WJZZY	This IC is based on LCD Driver and nano Watt Technology and is RISC microprocessor to control peripheral functions necessary for the system configuration. In this equipment, the R/C LED on the AVC side and system on the display side are controlled.
IC2301 5	RS232C Transmitters/ Receivers	VHIISL83220-1Y	This IC is a line driver receiver in conformity with EIA/TIA-232-E (former RS-232C) standard. By connecting a PC, the system can be controlled externally.
IC1710 6	CPLD	RH-IXB823WJZZQ	This IC is a CPLD of Altera and use CMOS EEPROM cells to implement logic functions with 64 Macrocells. This device controls ON/OFF power supply and signals for inverter unit.
IC1706 6	Stepdown Converter	VHIMP1410ES-1Y	The MP1410 is a monolithic step down switch mode regulator with a built in internal power MOSFET. In this model, it is assumed 1.8V DC/DC-CONVERTER and is used.
IC3001	E2PROM	VHIBR24L64F-1Y	The BR24L64F is a 2-wire (I2C bus type) serial EEPROM that is electrically programmable. This IC saves adjustment values of the adjustment process mode, etc. The data is given out by commands from the main microprocessor.
IC1901	E2PROM	VHI24LC2BIN-1Y	This IC is a 2-wire (I2C bus type) serial EEPROM this is electrically programmable. This EEPROM chip stores EDID data of the input for HDMI. This data is controlled by the I2C signal.
IC2303	E2PROM	VHIBR24C21F-1Y	This IC is a 2-wire (I2C bus type) serial EEPROM this is electrically programmable. This EEPROM chip stores EDID data of the input for PC. This data is controlled by the I2C signal.
KD604FM (AV UNIT)			
IC301 IC302	Sound Amp	VHITDA8931T-1Y	The TDA8931 is a switching power stage for high efficiency class-D audio power amplifier systems. With this amplifier a compact 1x 20 W closed loop self-oscillating digital amplifier system can be built. In this model, Audio amplifier is 10watt.
KD605FM (POWER UNIT)			
IC705	Switching Regulator	VHIMR4020++-1	This IC is a power supply for the switching regulator on the primary side. Overvoltage/overcurrent protection circuit, other protection circuits and control circuits are built in this IC.

Ref No.	Name	Part Code	Description
IC704	Switching Regulator	VHIMR4030++-1	This IC is a power supply for the switching regulator on the primary side. Overvoltage/overcurrent protection circuit, other protection circuits and control circuits are built in this IC.
KD628FM (DIDGITAL UNIT)			
IC4001 1	DTV-PROCES-SOR	RH-IXB680WJZZQ	This is a video/audio signal processing IC (Digital Processor) (STi5516) for digital tuner, which has been manufactured by STMicroelectronics, and incorporates a CPU. In this equipment, it implements GUI processing and video/audio processing for digital tuner, negotiation processing with CI-CARD, etc.
IC4201 2	64M-SDRAM	RH-IXB472WJZZQ	This IC is 64Mb SDRAM (static dynamic random-access memory) IC. In this equipment, it is used for SMI memory (for image processing), and data is used for operation of the digital processor.
IC4202 2	64M-SDRAM	RH-IXB472WJZZQ	This IC is 64Mb SDRAM (static dynamic random-access memory) IC. In this equipment, it is used for EMI memory (generally for CPU), and data is used for operation of the digital processor.
IC4203 2	16Mbit-FLASH	RH-IXB681WJZZQ	This IC is a high performance CMOS super technology 16Mbit Flash Memory. Start software (loader) for the CPU with a built-in digital processor and application software have been written on this Flash Memory. The digital processor reads these softwares on start-up and implements them.
IC4402/05	RATCH3 STATE	VHILVC573AP-1Y	This is a RATCH-3 STATE output IC. In this equipment, it is used to establish negotiation communication with CI-CARD.
IC4401 3	BALANCE TRANCEIVER	VHITCLCX245-2Y	This IC is a low voltage (3.3V) CMOS 8bit bidirectional transceiver. When setting the transmission direction change input DIR to ”H”, the A bus is switched to input and the B bus is changed to output; if the DIR is set to “L”, the B bus is switched to input and the A bus is changed to output. When setting the enable input OE to “H”, both A and B buses enter the high impedance state. In this equipment, it used to switch bus of the data from CICARD.
IC4404 3	Buffer/Line Driver	VHILCX244MT-1Y	This IC is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation. In this equipment, it is used to control negotiation communication with CI-CARD.
IC4604 4	3-OP-AMP	VHITSH73CPT	This IC is a Triple operational amplifiers featuring high video performances with large bandwidth, low distortion and excellent supply voltage rejection. In this equipment, it is used to convert audio output signal of the digital processor to normal analog signal level and to buffer it.
KD609FM (D-TUNER UNIT)			
IC201	IF-Demodurator/ PLL	VHITDA9886+-1Y	The TDA9886 is an alignment-free multistandard (PAL, SECAM and NTSC) vision and sound IF signal PLL demodulator for positive and negative modulation in cluding sound AM and FM processing.
IC202	COFDM Demod IC	RH-IXB682WJZZQ	This is a COFDM (Coded Orthogonal Frequency Division Multiplex) Demodulator IC. In this equipment, IF signal from the digital tuner is decoded to MPEG-2 signal, and it is digitally output. Output signal is fed to the digital processor to implement video/audio decode processing. This IC is used for digital signal is fed to the digital processor to implement video/audio decode processing. This IC is used for digital tuner only.

2. Detailed ICs Information

2.1. IC1905 (VHISII9021+-1Q)

2.1.1 Block Diagram



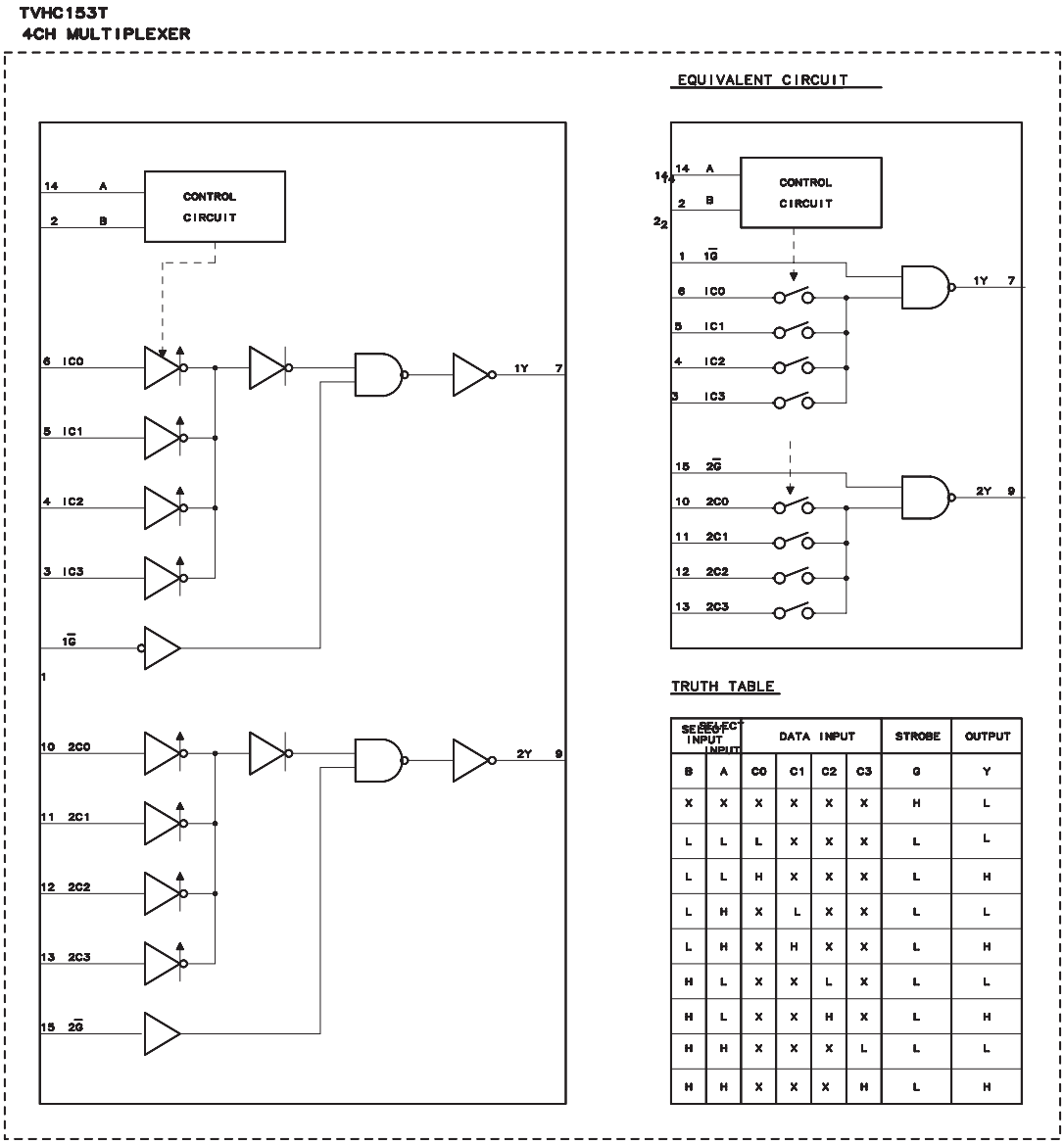
2.1.2 Pin Connections and short description

Pin No.	Pin Name	Type	Description
144	Q0	O	24-bit Output Pixel Data Bus.
143	Q1	O	24-bit Output Pixel Data Bus.
142	Q2	O	24-bit Output Pixel Data Bus.
141	Q3	O	24-bit Output Pixel Data Bus.
140	Q4	O	24-bit Output Pixel Data Bus.
137	Q5	O	24-bit Output Pixel Data Bus.
136	Q6	O	24-bit Output Pixel Data Bus.
133	Q7	O	24-bit Output Pixel Data Bus.
132	Q8	O	24-bit Output Pixel Data Bus.
131	Q9	O	24-bit Output Pixel Data Bus.
130	Q10	O	24-bit Output Pixel Data Bus.
129	Q11	O	24-bit Output Pixel Data Bus.
126	Q12	O	24-bit Output Pixel Data Bus.
125	Q13	O	24-bit Output Pixel Data Bus.
124	Q14	O	24-bit Output Pixel Data Bus.
123	Q15	O	24-bit Output Pixel Data Bus.
119	Q16	O	24-bit Output Pixel Data Bus.
118	Q17	O	24-bit Output Pixel Data Bus.
117	Q18	O	24-bit Output Pixel Data Bus.
116	Q19	O	24-bit Output Pixel Data Bus.
113	Q20	O	24-bit Output Pixel Data Bus.
112	Q21	O	24-bit Output Pixel Data Bus.
111	Q22	O	24-bit Output Pixel Data Bus.
110	Q23	O	24-bit Output Pixel Data Bus.
1	DE	O	Data enable.
2	HSYNC	O	Horizontal Sync Output control signal.
3	VSYNC	O	Vertical Sync Output control signal.
121	ODCK	O	Output Data Clock.
97	XTALIN	I	Crystal Clock Input.
96	XTALOUT	O	Crystal Clock Output.
88	MCLKOUT	O	Audio Master Clock Output.
87	MCLKIN	I	Audio Master Clock Input Reference.
86	SCK	O	I2S Serial Clock Output.
85	WS	O	I2S Word Select Output.
84	SDO	O	I2S Serial Data Output.
78	SPDIF	O	S/PDIF Audio Output.
77	MUTEOUT	O	Mute Audio Output.
104	INT	O	Interrupt Output.
102	RESET#	I	Reset Pin.Active LOW.
32	DSCLO	I	DDC I2C Clock for Port 0.
31	DSDAO	Bi-Di	DDC I2C Data for Port 0.
30	DSCL1	I	DDC I2C Clock for Port 1.
29	DSDA1	Bi-Di	DDC I2C Data for Port 1.
28	CSCL	I	Configuration I2C Clock.
27	CSDA	Bi-Di	Configuration I2C Data.
103	SCDT	O	Indicates active video at HDMI input port.
107	CLK48B	Bi-Di	Data Bus Latch Enable.
34	R0PWR5V	I	Port 0 Transmitter Detect.
33	R1PWR5V	I	Port 1 Transmitter Detect.
101	RSVDL	I	Reserved, must be tied LOW.
56	RSVD_A		Reserved Pin, leave unconnected.
93100	NC	–	No connect.
9	VREF	–	
81,82,83	RSVD	O	
14	AnRPr	O	Analog Video Red, Pr Output.
17	AnGY	O	Analog Video Green, Y Output.
20	AnBPb	O	Analog Video Blue, Pb Output.
11	COMP	–	Compensation. Provides compensation for the DAC's internal reference amplifier. This pin should be connected through capacitors to DACVCC externally. These capacitors must be close to the pin as possible to avoid any noise pick-up.
10	RSET	–	Full Scale Adjust Resistor. A precision(1%)resistor connected between this pin and DACGND controls the magnitude of the full scale video signal/RESET may need to be ajusted for optimum gain. This resistor must be as close to the pin as possible to avoid any noise pick-up.

Pin No.	Pin Name	Type	Description
40	R0XC+	I	TMDS input clock pair. HDMI Port 0
39	R0XC-	I	TMDS input clock pair. HDMI Port 0
44	R0X0+	I	TMDS input data pair. HDMI Port 0
43	R0X0-	I	TMDS input data pair. HDMI Port 0
48	R0X1+	I	TMDS input data pair. HDMI Port 0
47	R0X1-	I	TMDS input data pair. HDMI Port 0
52	R0X2+	I	TMDS input data pair. HDMI Port 0
51	R0X2-	I	TMDS input data pair. HDMI Port 0
59	R1XC+	I	TMDS input clock pair. HDMI Port 1
58	R1XC-	I	TMDS input clock pair. HDMI Port 1
63	R1X0+	I	TMDS input data pair. HDMI Port 1
62	R1X0-	I	TMDS input data pair. HDMI Port 1
67	R1X1+	I	TMDS input data pair. HDMI Port 1
66	R1X1-	I	TMDS input data pair. HDMI Port 1
71	R1X2+	I	TMDS input data pair. HDMI Port 1
70	R1X2-	I	TMDS input data pair. HDMI Port 1
23,79,92, 105,114, 128,139	CVCC18	–	Digital Logic VCC.
24,80,91, 106,115, 127,138	CGND	–	Digital Logic GND.
5,26,76,89, 109,122, 134	IOVCC	–	Input/Output Pin VCC.
4,25,75, 90,108, 120,135	IOGND	–	Input/Output Pin GND.
38,42,46, 50,57,61, 65,69	AVCC	–	TMDS Analog VCC.
41,45,49, 53,60,64, 68,72	AGND	–	TMDS Analog GND.
37	PVCC0	–	TMDS Port 0 PLL VCC.
55	PVCC1	–	TMDS Port 1 PLL VCC.
54	TMDSPGND	–	TMDS PLL GND.
13	DACVCCR	–	DAC Red VDD.
12	DACGNDR	–	DAC Red GND.
16	DACVCCG	–	DAC Green VDD.
15	DACGNDG	–	DAC Green GND.
19	DACVCCB	–	DAC Blue VDD.
18	DACGNDB	–	DAC Blue GND.
6	DACOVCC	–	DAC Output VCC.
7	DACAVCC	–	DAC Analog VCC.
8	DACAGND	–	DAC Analog GND.
22	DACVCC18	–	DAC Digital VCC.
21	DACGND	–	DAC Digital GND.
94	AUDPVCC18	–	ACR PLL VCC.
95	AUDPGND	–	ACR PLL GND.
35,74	DVCC18	–	ACR PLL Digital VCC.
36,73	DGND	–	ACR PLL GND.
98	XTALVCC	–	ACR PLL Crystal Input VCC.
99	REGVCC	–	ACR PLL Regulator VCC.

2.2. IC2701 (VHITVHC153T-1Y)

2.2.1 Block Diagram



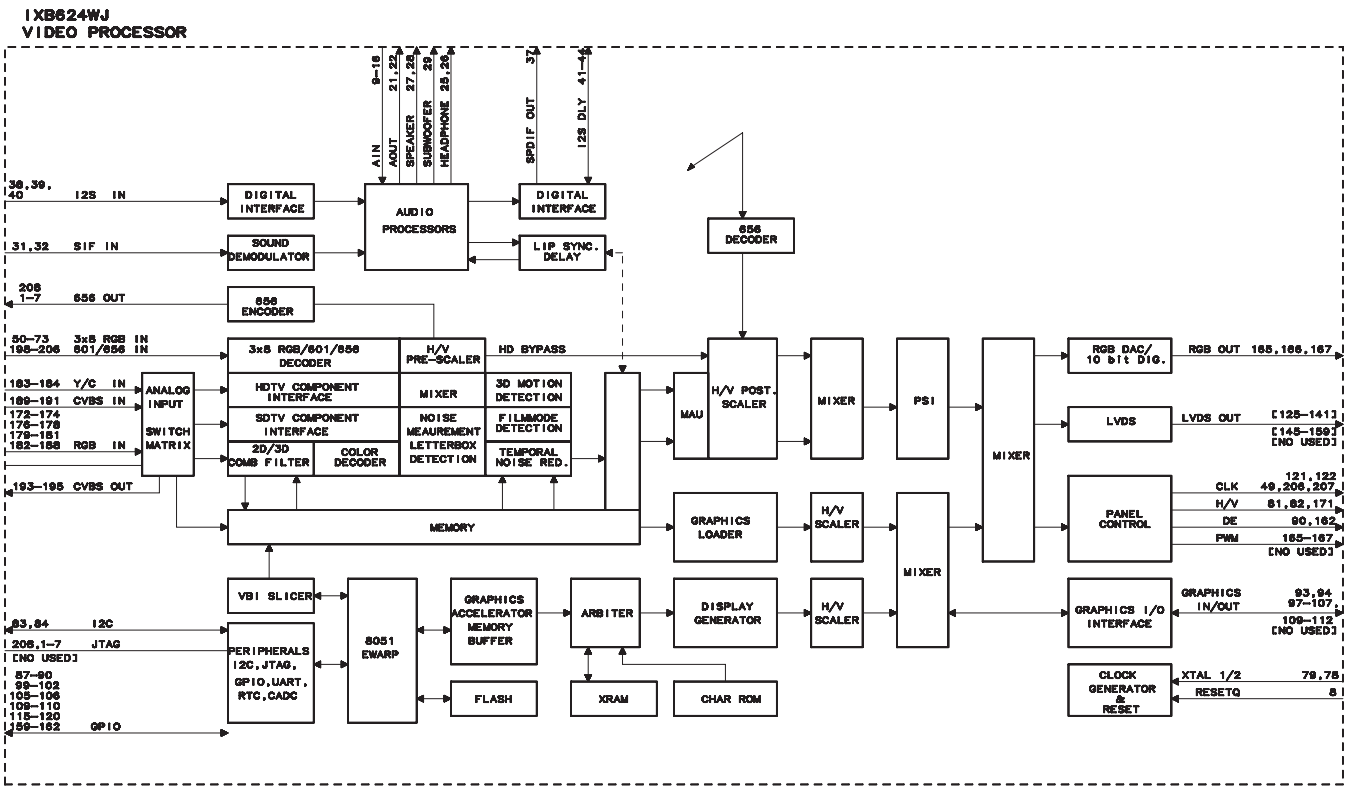
SELECT INPUT		DATA INPUT				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

2.2.2 Pin Connections and short description

Pin No.	Pin Name	I/O	Pin Function
1	$\overline{1G}$	I	Strobe input 1G.
2	B	I	Address input B.
3	1C3	I	Channel input 1C3.
4	1C2	I	Channel input 1C2.
5	1C1	I	Channel input 1C1.
6	1C0	I	Channel input 1C0.
7	1Y	O	Output signal 1Y.
8	GND	–	Ground.
9	2Y	O	Output signal 2Y.
10	2C0	I	Channel input 2C0.
11	2C1	I	Channel input 2C1.
12	2C2	I	Channel input 2C2.
13	2C3	I	Channel input 2C3.
14	A	I	Address input A.
15	$\overline{2G}$	I	Strobe input 2G
16	VCC	–	Power Source.

2.3. IC3002 (RH-IXB624WJN1Q)

2.3.1 Block Diagram



2.3.2 Pin Connections and short description

Pin No.	Pin Name	I/O	Pin Function	Sheet Name
1	656O6	O	Digital 656 Bit 6 Output	FRCI [6]
2	656O5	O	Digital 656 Bit 5 Output	FRCI [5]
3	656O4	O	Digital 656 Bit 4 Output	FRCI [4]
4	656O3	O	Digital 656 Bit 3 Output	FRCI [3]
5	656O2	O	Digital 656 Bit 2 Output	FRCI [2]
6	656O1	O	Digital 656 Bit 1 Output	FRCI [1]
7	656O0	O	Digital 656 Bit 0 Output (LSB)	FRCI [0]
8	RESETQ	I/O	Reset Input/Output	RESET-N
9	AIN1R	I	Analog Audio 1 Input, Right	AUDIO2_R
10	AIN1L	I	Analog Audio 1 Input, Left	AUDIO2_L
11	AIN2R	I	Analog Audio 2 Input, Right	EXT2 A_IN_R
12	AIN2L	I	Analog Audio 2 Input, Left	EXT2_A_IN_L
13	AIN3R	I	Analog Audio 3 Input, Right	EXT1 A_IN_R
14	AIN3L	I	Analog Audio 3 Input, Left	EXT1 A_IN_L
15	AIN4R	I	Analog Audio 4 Input, Right	EXT3 A_IN_R
16	AIN4L	I	Analog Audio 4 Input, Left	EXT3 A_IN_L
17	VREFAU	–	Reference Voltage, Audio	–
18	VSUP8.0AU	–	Supply Voltage Analog Audio, 8.0 V	S8V
19	GNDA	–	Ground Analog Audio, Platform Ground	GND
20	SGND	–	Analog Signal GND	GND
21	AOUT2R	O	Analog Audio 2 Output, Right	OUT2_R
22	AOUT2L	O	Analog Audio 2 Output, Left	OUT2_L
23	AOUT1R	O	Analog Audio 1 Output, Right	OUT1_R
24	AOUT1L	O	Analog Audio 1 Output, Left	OUT1_L
25	HEADPHONER	O	Analog Headphone Output, Right	open
26	HEADPHONEL	O	Analog Headphone Output, Left	open
27	SPEAKERR	O	Analog Loudspeaker Output, Right	SPK_OUT_R
28	SPEAKERL	O	Analog Loudspeaker Output, Left	SOK_OUT_L
29	SUBWOOFER	I/O	Analog SUBWOOFER Output	SBW_TEST
30	VREFSIF	ANA	Reference Voltage, Audio SIF	–

Pin No.	Pin Name	I/O	Pin Function	Sheet Name
31	SIFIN+	I	Differential Sound IF Input	SIF
32	SIFIN-	I	Differential Sound IF Input	–
33	VSUP5.0	–	Supply Voltage Analog, 5.0 V	+5V
34	GNDA	–	Ground Analog, Platform Ground	GND
35	GND3.3DIG	–	Ground Digital Interfaces	GND
36	VSUP3.3DIG	–	Supply Voltage Digital Interfaces, 3.3 V	3.3V
37	SPDIF_OUT	O	SPDIF Output	open
38	I2S_DA_IN	I	Audio Bus Data Input	I2S_D1
39	I2S_CL	I	Audio Bus Clock Input	A2S-CL
40	I2S_WS	I	Audio Bus Word Strobe Input	I2S_WS
41	I2S_DEL_OUT	I/O	Audio Delay Line Bus Data Output/Input	open
42	I2S_DEL_IN	I/O	Audio Delay Line Bus Data Input/Output	open
43	I2S_DEL_CL	I/O	Audio Delay Line Bus Clock Output/Input	open
44	I2S_DEL_WS	I/O	Audio Delay Line Word Strobe Output/Input	open
45	VSUP3.3RAM	–	Supply Voltage Ram, 3.3 V	3.3V
46	GND3.3RAM	–	Ground Ram	GND
47	DVS	I	Digital or Analog Video VSYNC HD Input	DVSYNC
48	DEN	I	Digital or Analog Video VSYNC HD Input	DINEN
49	DCLK	I	Digital Video Clock Input	DINCK
50	DRI7	I	Digital Video Red 7 Input	DINR [7]
51	DRI6	I	Digital Video Red 6 Input	DINR [6]
52	DRI5	I	Digital Video Red 5 Input	DINR [5]
53	DRI4	I	Digital Video Red 4 Input	DINR [4]
54	DRI3	I	Digital Video Red 3 Input	DINR [3]
55	DRI2	I	Digital Video Red 2 Input	DINR [2]
56	DRI1	I	Digital Video Red 1 Input	DINR [1]
57	DRI0	I	Digital Video Red 0 Input (LSB)	DINR [0]
58	DGI7	I	Digital Video Green 7 Input	DING [7]
59	DGI6	I	Digital Video Green 6 Input	DING [6]
60	DGI5	I	Digital Video Green 5 Input	DING [5]
61	DGI4	I	Digital Video Green 4 Input	DING [4]
62	DGI3	I	Digital Video Green 3 Input	DING [3]
63	DGI2	I	Digital Video Green 2 Input	DING [2]
64	DGI1	I	Digital Video Green 1 Input	DING [1]
65	DGI0	I	Digital Video Green 0 Input (LSB)	DING [0]
66	DBI7	I	Digital Video Blue 7 Input	DINB [7]
67	DBI6	I	Digital Video Blue 6 Input	DINB [6]
68	DBI5	I	Digital Video Blue 5 Input	DINB [5]
69	DBI4	I	Digital Video Blue 4 Input	DINB [4]
70	DBI3	I	Digital Video Blue 3 Input	DINB [3]
71	DBI2	I	Digital Video Blue 2 Input	DINB [2]
72	DBI1	I	Digital Video Blue 1 Input	DINB [1]
73	DBI0	I	Digital Video Blue 0 Input (LSB)	DINB [0]
74	GND3.3DRI	–	Ground Digital Ram Interface	GND
75	VSUP3.3DRI	–	Supply Voltage Digital Ram Interface, 3.3 V	3.3V
76	GND3.3COM	–	Ground Common	GND
77	VSUP3.3COM	–	Supply Voltage Common, 3.3V	3.3V
78	XTALIN	I	Analog Crystal Input	X_IN
79	XTALOUT	O	Analog Crystal Output	X_OUT
80	CLKOUT	O	Digital 20MHz Clock Output	open
81	VSO	O	Vertical Sync Output, Frontend	open
82	HSO	O	Horizontal Sync Output, Frontend	open
83	SCL	I/O	I2C Bus Clock Input/Output	BU_SCL3
84	SDA	I/O	I2C Bus Data Input/Output	BU_SDA3
85	GND3.3FL	–	Ground Flash	GND
86	VSUP3.3FL	–	Supply Voltage Flash, 3.3 V	3.3V
87	P2_0	I/O	Port 2, Bit 0 Input/Output	AVLK1
88	P2_1	I/O	Port 2, Bit 1 Input/Output	AVLK2
89	P2_2	I/O	Port 2, Bit 2 Input/Output	IRIN
90	P2_3	I/O	Port 2, Bit 3 Input/Output	KEY-PSW
91	P2_4	I/O	Port 2, Bit 4 Input/Output	TXD
92	P2_5	I/O	Port 2, Bit 5 Input/Output	RXD
93	OSDV	I/O	Graphic Vertical Sync Input/Output	open
94	OSDH	I/O	Graphic Horizontal Sync Input/Output	open

Pin No.	Pin Name	I/O	Pin Function	Sheet Name
95	GND3.3IO1	–	Ground Digital Input/Output Port 1	GND
96	VSUP3.3IO1	–	Supply Voltage Input/Output Port 1, 3.3 V	3.3V
97	OSDCLK	I/O	Graphic Clock Input/Output	open
98	OSDFSW	I/O	Graphic Fast Switch Input/Output	open
99	P3_7	I/O	Port3,bit7 Input/Output	HP JSW (HP PLUG)
100	P3_6	I/O	Port3,bit6 Input/Output	HOTP_CONT1
101	P3_5	I/O	Port3,bit5 Input/Output	HOTP_CONT0
102	P3_4	I/O	Port3,bit4 Input/Output	HDMI_INT
103	OSDB1	I/O	Graphic Blue 1 Input/Output	open
104	OSDB0	I/O	Graphic Blue 0 Input/Output	open
105	P3_3	I/O	Port3,bit3 Input/Output	P3_3
106	P3_2	I/O	Port3,bit2 Input/Output	open
107	OSDG1	I/O	Graphic Green 1 Input/Output	open
108	OSDG0	I/O	Graphic Green 0 Input/Output	open
109	P3_1	I/O	Port3,bit1 Input/Output	BL_ERR
110	P3_0	I/O	Port3,bit0 Input/Output	DTM_IRQ
111	OSDR1	I/O	Graphic Red 1 Input/Output	open
112	OSDR0	I/O	Graphic Red 0 Input/Output (LSB)	Open
113	GND3.3IO1	–	Ground Digital Input/Output Port 1	GND
114	VSUP3.3IO1	–	Supply Voltage Input/Output Port 1, 3.3 V	3.3V
115	P2_7	I/O	Port2,bit7 Input/Output	FPGA_SDA
116	P2_6	I/O	Port2,bit6 Input/Output	FPGA_SCK
117	P4_1	I/O	Port4,bit1 Input/Output	FPGA_SDE
118	P4_0	I/O	Port4,bit0 Input/Output	SVIJSW
119	P4_3	I/O	Port4,bit3 Input/Output	HSYNC_OSC
120	P4_2	I/O	Port4,bit2 Input/Output	VSYNC_OSC
121	PCLK2	O	Flat Panel Control Clock 2 Output	Open
122	PCLK1	O	Flat Panel Control Clock 1 Output	PCLK
123	GND1.8DIG	–	Ground Digital Core	GND
124	VSUP1.8DIG	–	Supply Voltage Digital Core, 1.8 V	1.8V
125	LVDSA_4P	O	LVDS Channel 1 bit 4 Positive Output 2)	Open
126	LVDSA_4N	O	LVDS Channel 1 bit 4 Negative Output 2)	Open
127	VSUP3.3LVDS	–	Supply Digital Voltage LVDS2) Port, 3.3 V	3.3V
128	LVDSA_3P	O	LVDS Channel 1 bit 3 Positive Output 2)	LVDS3P
129	LVDSA_3N	O	LVDS Channel 1 bit 3 Negative Output 2)	LVDS3N
130	GND3.3LVDS	–	Ground Digital LVDS2), 3.3 V	GND
131	LVDSA_CLKP	O	LVDS Channel 1 Clock Positive Output 2)	LVDSCP
132	LVDSA_CLKN	O	LVDS Channel 1 Clock Negative Output 2)	LVDSCN
133	VSUP3.3LVDS	–	Supply Digital Voltage LVDS2), 3.3 V	3.3V
134	LVDSA_2P	O	LVDS Channel 1 bit 2 Positive Output 2)	LVDS2P
135	LVDSA_2N	O	LVDS Channel 1 bit 2 Negative Output 2)	LVDS2N
136	GND3.3LVDS	–	Ground Digital LVDS2), 3.3 V	GND
137	LVDSA_1P	O	LVDS Channel 1 bit 1 Positive Output 2)	LVDS1P
138	LVDSA_1N	O	LVDS Channel 1 bit 1 Negative Output 2)	LVDS1N
139	VSUP3.3LVDS	–	Supply Digital Voltage LVDS2), 3.3 V	3.3V
140	LVDSA_0P	O	LVDS Channel 1 bit 0 Positive Output 2)	LVDS0P
141	LVDSA_0N	O	LVDS Channel 1 bit 0 Negative Output 2)	LVDS0N
142	VSUP1.8LVDS	–	Supply Analog Voltage LVDS2), 1.8 V	1.8V
143	REXT	–	LVDS External Resistor2)	REXT
144	GND1.8LVDS	–	Ground Analog LVDS2), 1.8 V	GND
145	LVDSB_3P	O	Dual-LVDS Channel 2 bit 3 Positive Output 2)	Open
146	LVDSB_3N	O	Dual-LVDS Channel 2 bit 3 Negative Output 2)	Open
147	GND3.3LVDS	–	Ground Digital LVDS2), 3.3 V	GND
148	LVDSBCLKP	O	Dual-LVDS Channel 2 Clock Positive Output 2)	Open
149	LVDSBCLKN	O	Dual-LVDS Channel 2 Clock Negative Output 2)	Open
150	VSUP3.3LVDS	–	Supply Digital Voltage LVDS2), 3.3 V	3.3V
151	LVDSB_2P	O	Dual-LVDS Channel 2 bit 2 Positive Output 2)	Open
152	LVDSB_2N	O	Dual-LVDS Channel 2 bit 2 Negative Output 2)	Open
153	GND3.3LVDS	–	Ground Digital LVDS2), 3.3 V	GND
154	LVDSB_1P	O	Dual-LVDS Channel 2 bit 1 Positive Output 2)	Open
155	LVDSB_1N	O	Dual-LVDS Channel 2 bit 1 Negative Output 2)	Open
156	VSUP3.3LVDS	–	Supply Digital Voltage LVDS2), 3.3 V	3.3V
157	LVDSB_0P	O	Dual-LVDS Channel 2 bit 0 Positive Output 2)	Open
158	LVDSB_0N	O	Dual-LVDS Channel 2 bit 0 Negative Output 2)	Open

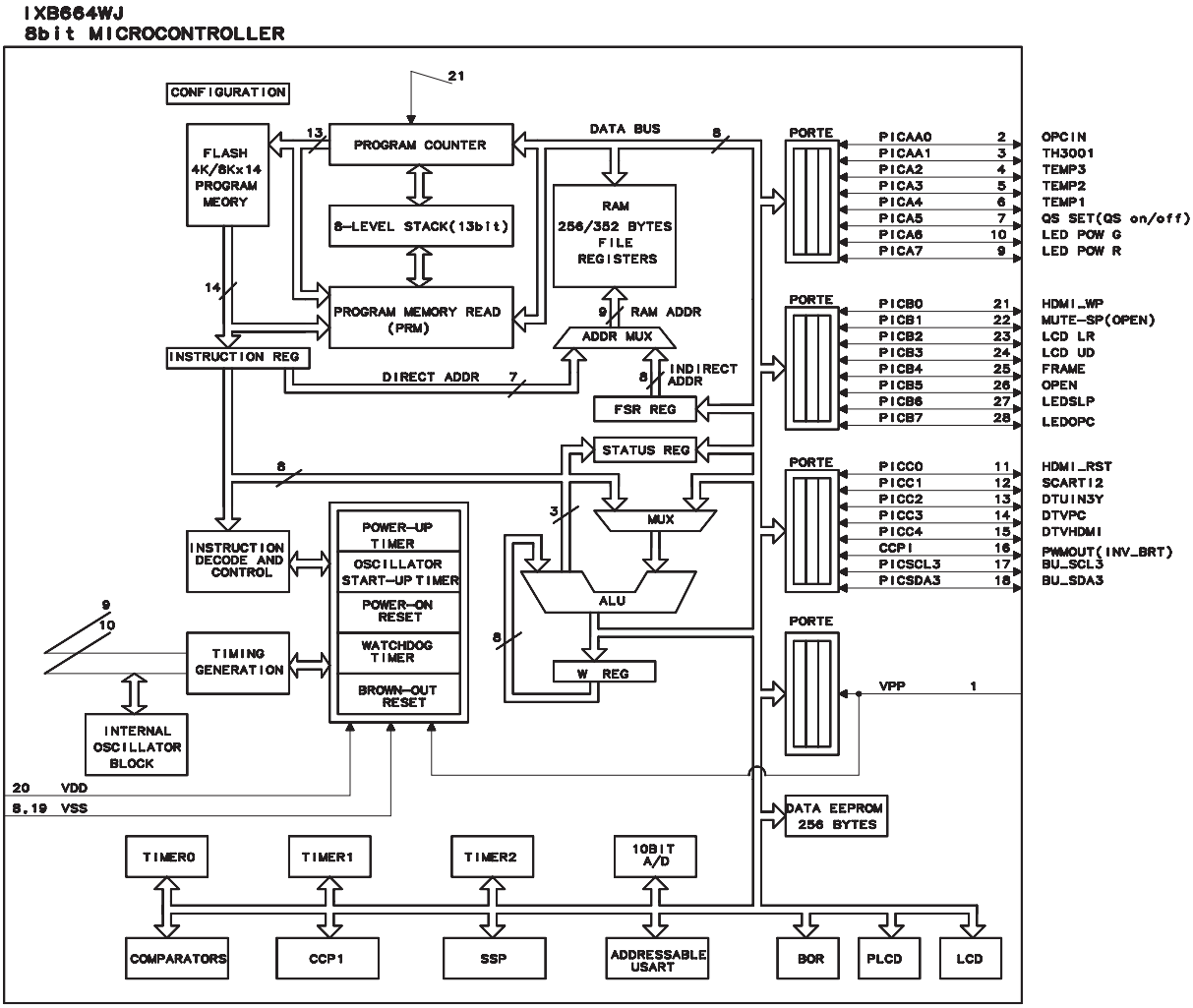
Pin No.	Pin Name	I/O	Pin Function	Sheet Name
159	P1_7	I/O	Port 1, Bit 7 Input/Output	IF_AGC
160	P1_6	I/O	Port 1, Bit 6 Input/Output	SLOW SW1
161	P1_5	I/O	Port 1, Bit 5 Input/Output	SLOW SW2
162	P1_4	I/O	Port 1, Bit 4 Input/Output	KEY_ETC
163	GND3.3DAC	–	Ground DAC	GND
164	VSUP3.3DAC	–	Supply Voltage DAC, 3.3V	3.3V
165	P1_3	I/O	Port 1, Bit 3 Input/Output	Open
166	P1_2	I/O	Port 1, Bit 2 Input/Output	Open
167	P1_1	I/O	Port 1, Bit 1 Input/Output	Open
168	P1_0	I/O	Port 1, Bit 0 Input/Output	Open
169	VSUP1.8FE	–	Supply Voltage Analog Video Frontend, 1.8 V	1.8V
170	VSUP3.3FE	–	Supply Voltage Analog Video Frontend, 3.3 V	3.3V
171	DHS	I	Digital Video H-sync Input	DHSYNC
172	VIN21	I	Analog Video 21B HD Input	PC_V_B
173	VIN20	I	Analog Video 20 G HD Input	PC_V_G
174	VIN19	I	Analog Video 19 R HD Input	PC_V_R
175	VIN18	I	Analog Video 18 Fast Blank 2 Input	IN2_FSW
176	VIN17	I	Analog Video 17 B HD Input	BLUE2
177	VIN16	I	Analog Video 16 G HD Input	GREEN2
178	VIN15	I	Analog Video 15 R HD Input	RED/C2
179	VIN13	I	Analog Video 13 B HD Input	D TUNER_B
180	VIN12	I	Analog Video 12 G HD Input	D_TUNER_G
181	VIN11	I	Analog Video 11 R HD Input	D_TUNER_R
182	VIN9	I	Analog Video 9 Y or B SD Input	BLUE1
183	VIN8	I	Analog Video 8 C or Fast Blank 1 Input	IN3C
184	VIN7	I	Analog Video 7 Y or G SD Input	IN3Y
185	VSUP1.8FE	–	Supply Voltage Analog Video Frontend, 1.8 V	1.8V
186	VSUP1.8FE	–	Analog Video Frontend, Platform Ground	GND
187	VIN6	I	Analog Video 6 C or R SD Input	RED/C1
188	VIN5	I	Analog Video 5 Y/CVBS Input	GREEN1
189	VIN3	I	Analog Video 3 CVBS Input	IN1_FSW
190	VIN2	I	Analog Video 2 CVBS Input	VIN_2
191	VIN1	I	Analog Video 1 CVBS Input	A_TUNER_CVBS
192	VSUP3.3VO	–	Supply Voltage Analog Video Output, 3.3 V	3.3V
193	VOUT3	O	Analog CVBS Video 3 Output	Open
194	VOUT2	O	Analog CVBS Video 2 Output	CV02 (outV)
195	VOUT1	O	Analog CVBS Video 1 Output	CV01 (outNV)
196	GND3.3IO3	–	Ground Digital Input/Output Port 1	GND
197	VSUP3.3IO3	–	Supply Voltage Input/Output Port 1, 3.3 V	3.3V
198	656I0	I	Digital 656 Bit 0 Input (LSB)	FRCO [0]
199	656I1	I	Digital 656 Bit 1 Input	FRCO [1]
200	656I2	I	Digital 656 Bit 2 Input	FRCO [2]
201	656I3	I	Digital 656 Bit 3 Input	FRCO [3]
202	656I4	I	Digital 656 Bit 4 Input	FRCO [4]
203	656I5	I	Digital 656 Bit 5 Input	FRCO [5]
204	656I6	I	Digital 656 Bit 6 Input	FRCO [6]
205	656I7	I	Digital 656 Bit 7 Input	FRCO [7]
206	656CLKI	I	Digital 656 Clock Input	FRCCKO
207	656CLKO	O	Digital 656 Clock Output	FRCCKI
208	656O7	O	Digital 656 Bit 7 Output	FRCI [7]

1) TTL output version only

2) LVDS output version only

2.4. IC3003 (RH-IXB664WJZZY)

2.4.1 Block Diagram



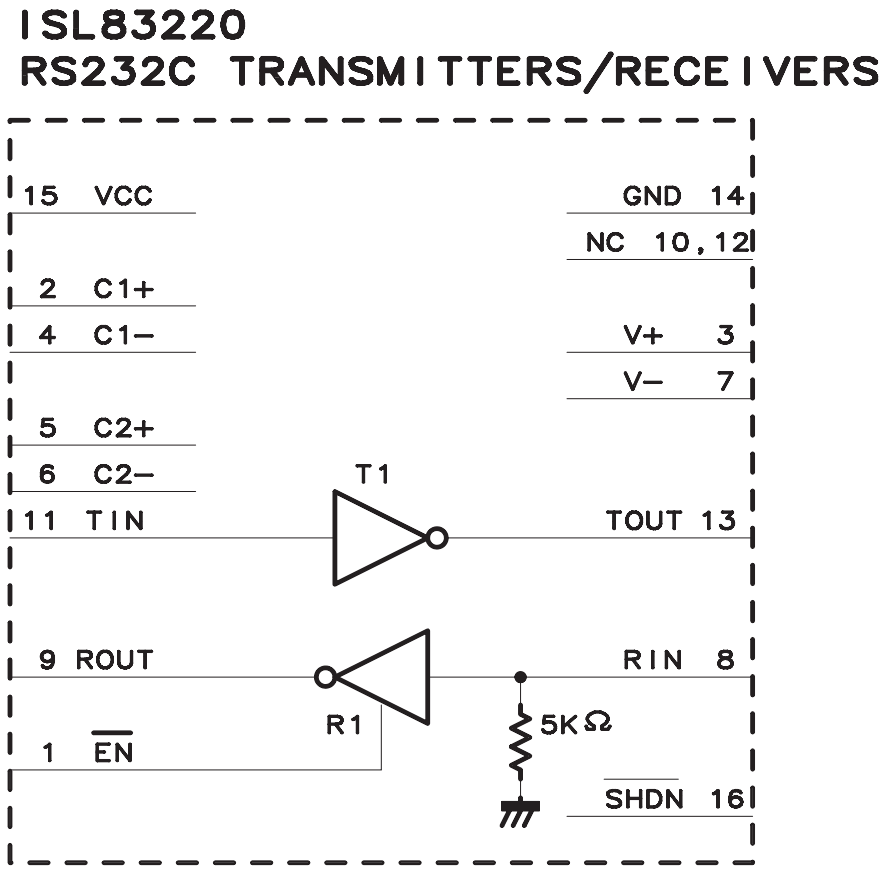
2.4.2 Pin Connections and short description

Pin No.	Pin Name	I/O	Pin Function	Sheet Name
2	PICAA0	I	OPC_in Signal.	OPCIN
3	PICAA1	I	Connect to TH3001.	TH3001
4	PICA2	O	TEM3 Signal.	TEMP3
5	PICA3	O	TEMP2 Signal.	TEMP2
6	PICA4	O	TEMP1 Signal.	TEMP1
7	PICA5	O	QS' on/off Signal.	QS SET (QS on/off)
10	PICA6	I	LED Power Green Signal.	LED POW G
9	PICA7	I	LED Power Red Signal.	LED POW R
21	PICBO	O	HDMI_Write Protect Signal.	HDMI_WP
22	PICB1	O	Mute_SP Signal.	MUTE-SP (Open)
23	PICB2	O	LCD, S_LBR Signal.	LCD LR
24	PICB3	O	LCD, G_LBR Signal.	LCD UD
25	PICB4	O	50/60Hz Ds_Select Signal.	FRAME
26	PICB5	–	–	Open
27	PICB6	I	LED Sleep LED IN Signal.	LEDSLP
28	PICB7	I	LED OPC IN Signal.	LED OPC
11	PICCO	O	Reset Signal to HDMI.	HDMI_RST
12	PICC1	O	SCART1/SCART2 Select Signal.	SCART12
13	PICC2	O	DTU/IN3Y Select Signal.	DTUIN3Y
14	PICC3	O	DTV/PC Select Signal.	DTVPC
15	PICC4	O	DTV/HDMI Select Signal.	DTVHDMI

Pin No.	Pin Name	I/O	Pin Function	Sheet Name
16	CCPI	O	INVERTER_BRT Signal.	PWMOUT (INV_BRT)
17	PICSCL3	I/O	I2C clock.	BU_SCL3
18	PICSDA3	I/O	I2C data.	BU_SDA3
1	VPP	–	Open	Open
20	3.3V	–	Power Supply for microcontroller	VSUP3.3DRI
8, 19	GND	–	Ground reference for microcontroller	GND

2.5. IC2301 (VHIISL83220-1Y)

2.5.1 Block Diagram

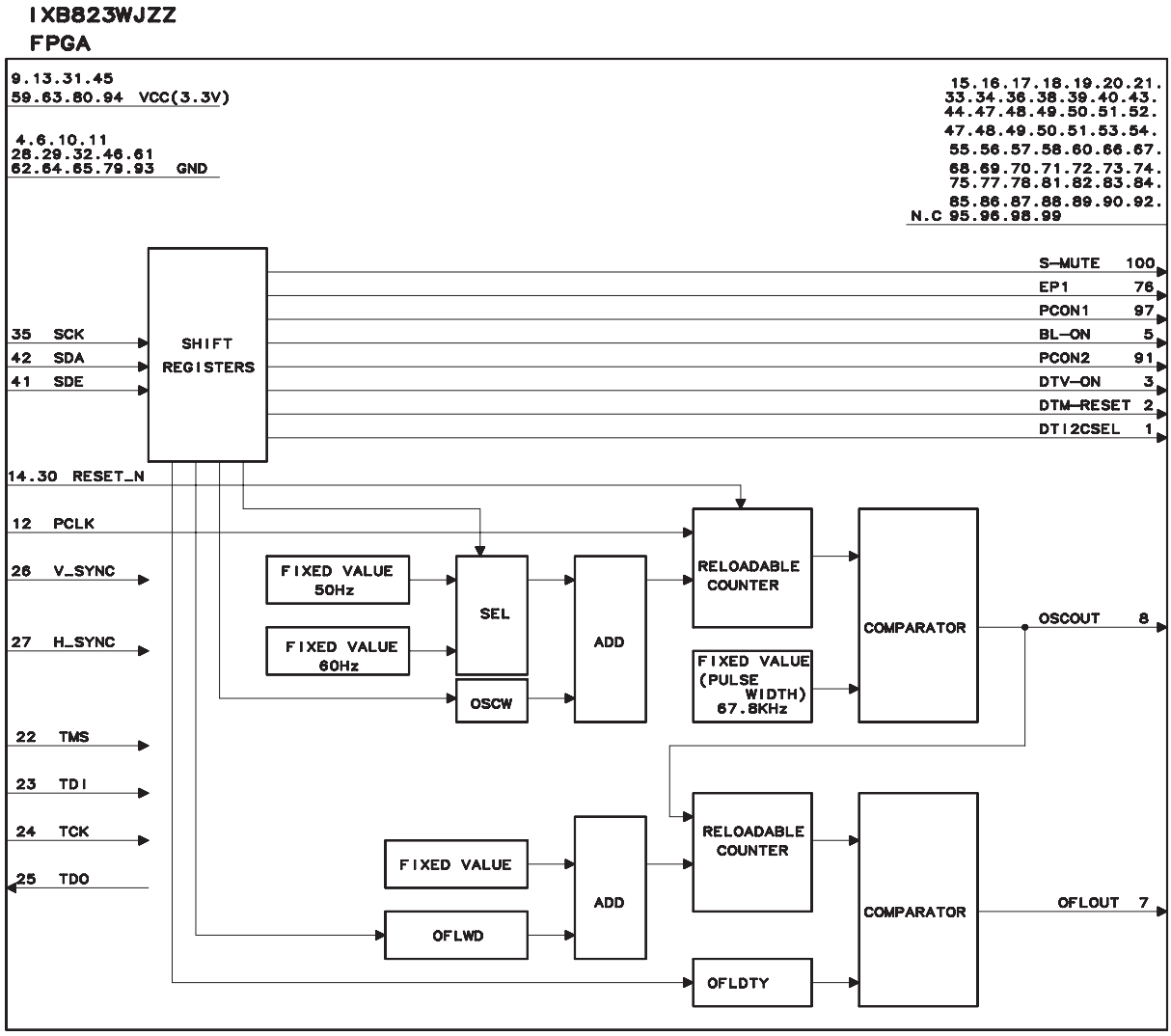


2.5.2 Pin Connections and short description

Pin No.	Pin Name	I/O	Pin Function
15	VCC	–	System power supply input (3.0V to 5.5V).
3	V+	–	Intemally generated positive transmitter supply (+5.5V).
7	V-	–	Internally generated negative transmitter supply (-5.5V).
14	GND	–	Ground connection.
2	C1+	–	External capacitor (voltage doubler) is connected to this lead.
4	C1-	–	External capacitor (voltage doubler) is connected to this lead.
5	C2+	–	External capacitor (voltage doubler) is connected to this lead.
6	C2-	–	External capacitor (voltage doubler) is connected to this lead.
11	TIN	I	TTL/CMOS compatible transmitter inputs.
13	TOUT	O	±15KV ESD Protected, RS-232 level (nominally ±5.5V) transmitter output.
8	RIN	I	±15KV ESD Protected, RS-232 compatible receiver inputs.
9	ROUT	O	TTL/CMOS level receiver output.
1	$\overline{EN}$	O	Active low receiver enable control; doesn't disable ROUTB output.
16	$\overline{SHDN}$	–	Active low input shuts down transmitters and on-board power supply, to place device in low power mode.
10	N.C.	–	No internal connection.

2.6. IC1710 (RH-IXB823WJZZQ)

2.6.1 Block Diagram



2.6.2 Pin Connections and short description

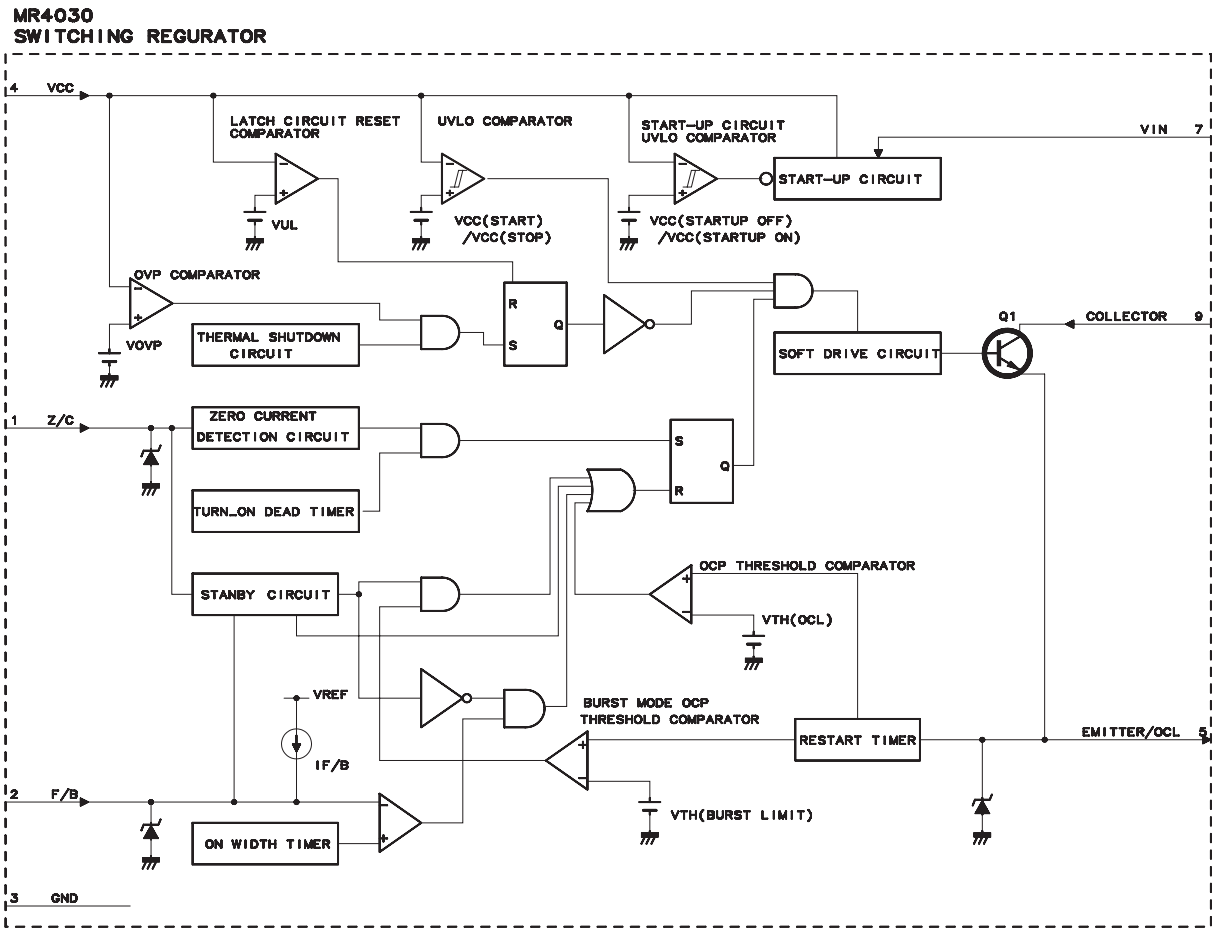
Pin No.	Pin Name	I/O	Pin Function	NET_NAME
1	EXP [7]	O	Outport [7]	DTI2CSEL
2	EXP [6]	O	Outport [6]	DTM_RESET
3	EXP [5]	O	Outport [5]	DTV_ON
4	GND*	–	Ground	N.C.
5	EXP [3]	O	Outport [3]	BL_ON
6	GND*	–	Ground	N.C.
7	OFLOUT	O	OFL signal output	OFLOUT
8	OSCOUT	O	OSC signal output	OSCOUT
9	VCCIO1	–	VCC (3.3V)	FPGA_VCC
10	GNDIO	–	Ground	Ground.
11	GNDINT	–	ground.	Ground.
12	PCLK	I	Reference clock input	PCLK
13	VCCINT	–	VCC (3.3V)	FPGA_VCC
14	GCLR	I	RESET terminal. L: RESET, H: Normal	RESET_N
15	GND*	–	N.C.	N.C.
16	GND*	–	N.C.	N.C.
17	GND*	–	N.C.	N.C.
18	GND*	–	N.C.	N.C.
19	GND*	–	N.C.	N.C.
20	GND*	–	N.C.	N.C.

Pin No.	Pin Name	I/O	Pin Function	NET_NAME
21	GND*	–	N.C.	N.C.
22	#TMS	I	Pin for JTAG write	FPGA_TMS
23	#TDI	I	Pin for JTAG write	FPGA_TDI
24	#TCK	I	Pin for JTAG write	FPGA_TCK
25	#TDO	O	Pin for JTAG write	FPGA_TDO
26	VSYNC	I	V sync input (not used)	V_SYNC
27	HSYNC	I	H sync input (not used)	H_SYNC
28	GND*	–	N.C.	N.C.
29	GND*	–	N.C	N.C.
30	DMY_IN	I	Dummy pin for RESET line wiring (no effect on operation)	RESET_N
31	VCCIO1	–	VCC (3.3V)	FPGA_VCC
32	GNDIO	–	Ground.	Ground.
33	GND*	–	N.C.	N.C.
34	GND*	–	N.C.	N.C.
35	SCK	I	Microprocessor control bus clock	SCK
36	GND*	–	N.C.	N.C.
37	GND*	–	N.C.	N.C.
38	GND*	–	N.C.	N.C.
39	GND*	–	N.C.	N.C.
40	GND*	–	N.C.	N.C.
41	SEN	I	Microprocessor control bus enable	SDE
42	SDA	I	Microprocessor control bus data	SDA
43	GND*	–	N.C.	N.C.
44	GND*	–	N.C.	N.C.
45	VCCIO1	–	VCC (3.3V)	FPGA_VCC
46	GNDIO	–	Ground.	Ground.
47	GND*	–	N.C.	N.C.
48	GND*	–	N.C.	N.C
49	GND*	–	N.C.	N.C.
50	GND*	–	N.C.	N.C.
51	GND*	–	N.C.	N.C.
52	GND*	–	N.C.	N.C.
53	GND*	–	N.C.	N.C.
54	GND*	–	N.C.	N.C.
55	GND*	–	N.C.	N.C.
56	GND*	–	N.C.	N.C.
57	GND*	–	N.C.	N.C.
58	GND*	–	N.C.	N.C.
59	VCCIO2	–	VCC (3.3V)	FPGA_VCC
60	GNDIO	–	Ground.	Ground.
61	GND*	–	Ground.	N.C.
62	GND*	–	Ground.	Ground.
63	VCCINT	–	VCC (3.3V)	FPGA_VCC
64	GND*	–	Ground.	Ground.
65	GNDINT	–	Ground.	Ground.
66	GND*	–	N.C.	N.C.
67	GND*	–	N.C	N.C.
68	GND*	–	N.C	N.C.
69	GND*	–	N.C	N.C.
70	GND*	–	N.C	N.C.
71	GND*	–	N.C	N.C.
72	GND*	–	N.C	N.C.
73	GND*	–	N.C	N.C.
74	GND*	–	N.C	N.C.
75	GND*	–	N.C	N.C.
76	EXP [1]	O	Outport [1]	EP1
77	GND*	–	N.C	N.C.
78	GND*	–	N.C.	N.C.
79	GNDIO	–	Ground.	Ground.
80	VCCIO2	–	VCC (3.3V)	FPGA_VCC
81	GND*	–	N.C.	N.C
82	GND*	–	N.C.	N.C
83	GND*	–	N.C.	N.C
84	GND*	–	N.C.	N.C

Pin No.	Pin Name	I/O	Pin Function	NET_NAME
85	GND*	–	N.C.	N.C
86	GND*	–	N.C.	N.C
87	GND*	–	N.C.	N.C
88	GND*	–	N.C.	N.C
89	GND*	–	N.C.	N.C
90	GND*	–	N.C.	N.C
91	EXP [4]	O	Outport [4]	PCON2 (EP4)
92	GND*	–	N.C.	N.C
93	GNDIO	–	Ground.	Ground.
94	VCCIO2	–	VCC (3.3V)	FPGA_VCC
95	GND*	–	N.C.	N.C
96	GND*	–	N.C.	N.C
97	EXP [2]	O	Outport [2]	PCON1 (EP2)
98	GND*	–	N.C	N.C
99	GND*	–	N.C.	N.C
100	EXP [0]	O	Outport [0]	S_MUTE

2.7. IC704 (VHIMR4030++-1)

2.7.1 Block Diagram



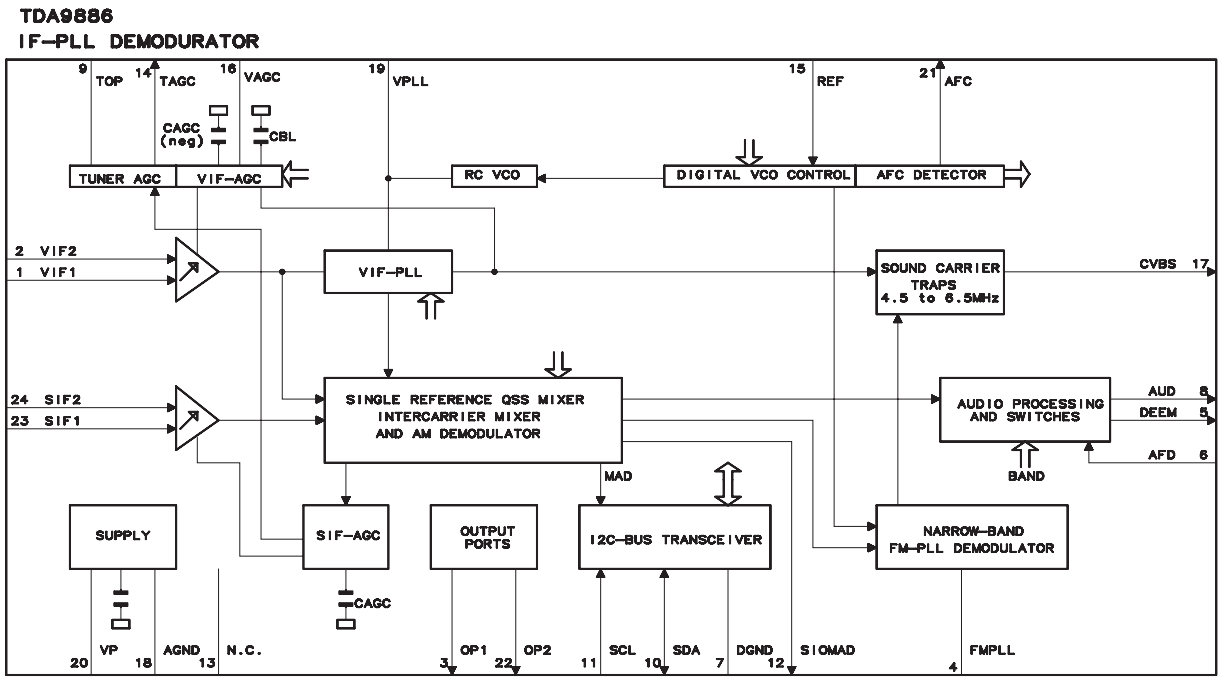
2.7.2 Pin Connections and short description

Pin No.	Pin Name	I/O	Pin Function
1	Z/C	I	Zero Current Detection Terminal.
2	F/B	I	Feed Back terminal.
3	GND	–	Ground Terminal.
4	VCC	–	VCC Terminal.
5	Emitter/OCL	O	Emitter/OCL terminal.

Pin No.	Pin Name	I/O	Pin Function
7	VIN	I	VIN Terminal.
8	Collector	I	Collector Terminal.

2.8. IC201 (VHITDA9886+-1Y)

2.8.1 Block Diagram



2.8.2 Pin Connections and short description

Pin No.	Pin Name	I/O	Pin Function
1	VIF1	I	VIF differential input 1
2	VIF2	I	VIF differential input 2
3	OP1	O	Output port 1; open-collector.
4	FMPLL	I	FM-PLL for loop filter.
5	DEEM	O	De-emphasis output for capacitor.
6	AFD	I	AF decoupling input for capacitor
7	DGND	–	Digital ground.
8	AUD	O	Audio output.
9	TOP	I	Tuner AGC TakeOver Pint (TOP) for resistor adjustment.
10	SDA	I/O	I2C-bus data input and output.
11	SCL	I	I2C-bus clock input.
12	SIOMAD	O	Sound intercarrier output and MAD select with resistor.
13	N.C.	–	Not connected.
14	TAGC	O	Tuner AGC output.
15	REF	I	4 MHz crystal or reference signal input.
16	VAGC(1)	I	VIF-AGC for capacitor.
17	CVBS	O	Composite video output.
18	AGND	–	Analog ground.
19	VPLL	I	VIF-PLL for loop filter.
20	VP	–	Supply voltage.
21	AFC	O	AFC output.
22	OP2	O	Output port 2; open-collector.
23	SIF1	I	SIF differential input 1 and MAD select with resistor.
24	SIF2	I	SIF differential input 2 and MAD select with resistor.